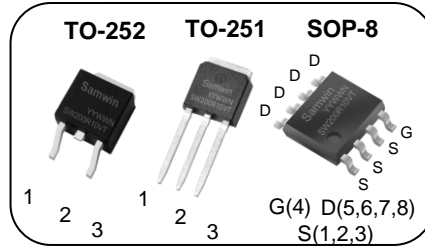


## N-channel Enhanced mode TO-252/TO-251/SOP-8 MOSFET

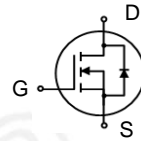
### Features

- High ruggedness
- Low  $R_{DS(ON)}$  (Typ 19.5m $\Omega$ )@ $V_{GS}=4.5V$   
(Typ 18.7m $\Omega$ )@ $V_{GS}=10V$
- Low Gate Charge (Typ 86nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: Synchronous Rectification, Li Battery Protect Board, Inverter.



TO-252/TO-251 : 1. Gate 2. Drain 3. Source  
SOP-8: 4. Gate 5,6,7,8. Drain 1,2,3. Source

$BV_{DSS}$	: 100V
$I_D$	: 36A
$R_{DS(ON)}$	: 19.5m $\Omega$ @ $V_{GS}=4.5V$ 18.7m $\Omega$ @ $V_{GS}=10V$



### General Description

This power MOSFET is produced with advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.



### Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW D 200R10VT	SW200R10VT	TO-252	REEL
2	SW I 200R10VT	SW200R10VT	TO-251	TUBE
3	SW K 200R10VT	SW200R10VT	SOP-8	REEL

### Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-252	TO-251	SOP-8	
$V_{DSS}$	Drain to source voltage	100			V
$I_D$	Continuous drain current (@ $T_C=25^\circ C$ )	36*			A
	Continuous drain current (@ $T_C=100^\circ C$ )	23*			A
$I_{DM}$	Drain current pulsed (note 1)	144			A
$V_{GS}$	Gate to source voltage	$\pm 20$			V
$E_{AS}$	Single pulsed avalanche energy (note 2)	72			mJ
$E_{AR}$	Repetitive avalanche energy (note 1)	11			mJ
dv/dt	Peak diode recovery dv/dt (note 3)	5			V/ns
$P_D$	Total power dissipation (@ $T_C=25^\circ C$ )	117	160		W
	Total power dissipation (@ $T_A=25^\circ C$ )			2.9	W
	Derating factor above 25 $^\circ C$	0.9	1.3	0.02	W/ $^\circ C$
$T_{STG}, T_J$	Operating junction temperature & storage temperature	-55 ~ + 150			$^\circ C$

\*. Drain current is limited by junction temperature.

### Thermal characteristics

Symbol	Parameter	Value			Unit
		TO-252	TO-251	SOP-8	
$R_{thjc}$	Thermal resistance, Junction to case	1.07	0.78		$^\circ C/W$
$R_{thja}$	Thermal resistance, Junction to ambient		73	43	$^\circ C/W$

Note:  $R_{thja}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{thjc}$  is guaranteed by design while  $R_{thca}$  is determined by the user's board design. SOP-8  $R_{thja}$  : 43 $^\circ C/W$  on a 1 in $^2$  pad of 2oz copper.

## Electrical characteristic ( $T_C = 25^\circ\text{C}$ unless otherwise specified )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Off characteristics</b>						
$BV_{DSS}$	Drain to source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	100			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=250\mu A$ , referenced to $25^\circ\text{C}$		0.07		$V/^\circ\text{C}$
$I_{DSS}$	Drain to source leakage current	$V_{DS}=100V, V_{GS}=0V$			1	$\mu A$
		$V_{DS}=80V, T_C=125^\circ\text{C}$			50	$\mu A$
$I_{GSS}$	Gate to source leakage current, forward	$V_{GS}=20V, V_{DS}=0V$			100	nA
	Gate to source leakage current, reverse	$V_{GS}=-20V, V_{DS}=0V$			-100	nA
<b>On characteristics</b>						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5		2.5	V
$R_{DS(ON)}$	Drain to source on state resistance(TO251&TO252)	$V_{GS}=4.5V, I_D=18A$		19.5	25	m $\Omega$
		$V_{GS}=10V, I_D=18A$		18.7	23	
		$V_{GS}=10V, I_D=36A$		19.1	24	
	Drain to source on state resistance(SOP8)	$V_{GS}=4.5V, I_D=18A$		22.8	28.5	
		$V_{GS}=10V, I_D=18A$		22.0	27.5	
$G_{fs}$	Forward transconductance	$V_{DS}=10V, I_D=18A$		77		S
<b>Dynamic characteristics</b>						
$C_{iss}$	Input capacitance	$V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$		4410		pF
$C_{oss}$	Output capacitance			165		
$C_{rss}$	Reverse transfer capacitance			153		
$t_{d(on)}$	Turn on delay time	$V_{DS}=50V, I_D=36A, R_G=25\Omega, V_{GS}=10V$ (note 4,5)		26		ns
$t_r$	Rising time			61		
$t_{d(off)}$	Turn off delay time			321		
$t_f$	Fall time			116		
$Q_g$	Total gate charge	$V_{DS}=80V, V_{GS}=10V, I_D=36A$ (note 4,5)		86		nC
$Q_{gs}$	Gate-source charge			15		
$Q_{gd}$	Gate-drain charge			20		
$R_g$	Gate resistance	$V_{DS}=0V$ , Scan F mode		1.5		$\Omega$

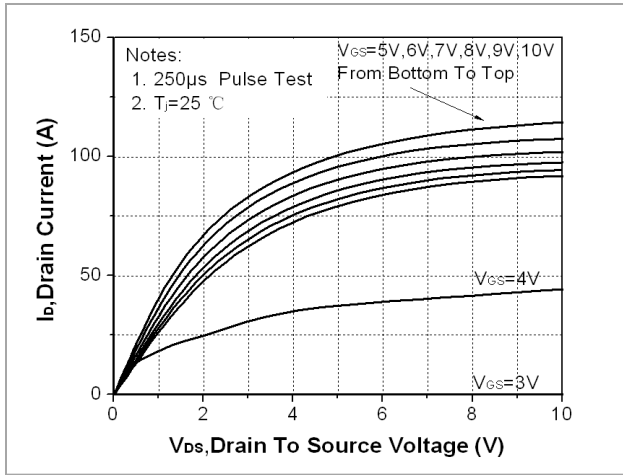
## Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			36	A
$I_{SM}$	Pulsed source current				144	A
$V_{SD}$	Diode forward voltage drop.	$I_S=36A, V_{GS}=0V$			1.4	V
$t_{rr}$	Reverse recovery time	$I_S=36A, V_{GS}=0V,$		42		ns
$Q_{rr}$	Reverse recovery charge	$di_f/dt=100A/\mu s$		70		nC

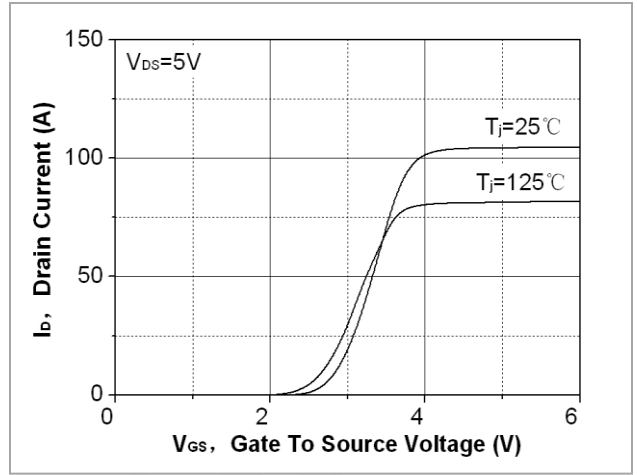
### ※. Notes

1. Repeattive rating : pulse width limited by junction temperature.
2.  $L=0.5\text{mH}, I_{AS}=17A, V_{DD}=50V, R_G=25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 36A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
5. Essentially independent of operating temperature.

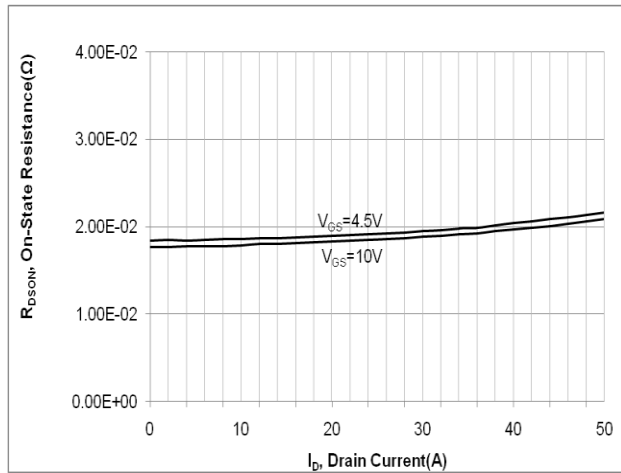
**Fig. 1. On-state characteristics**



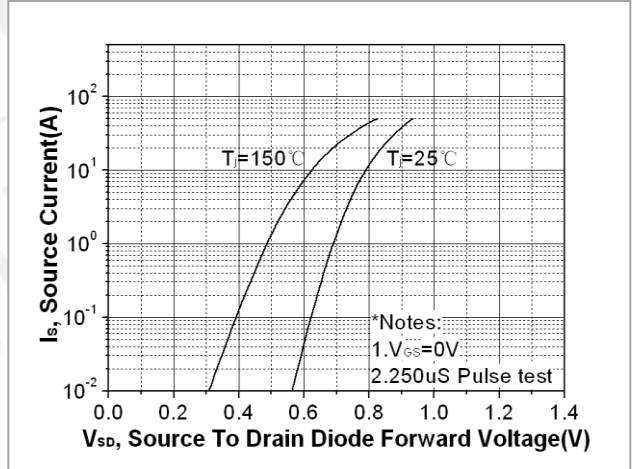
**Fig. 2. Transfer Characteristics**



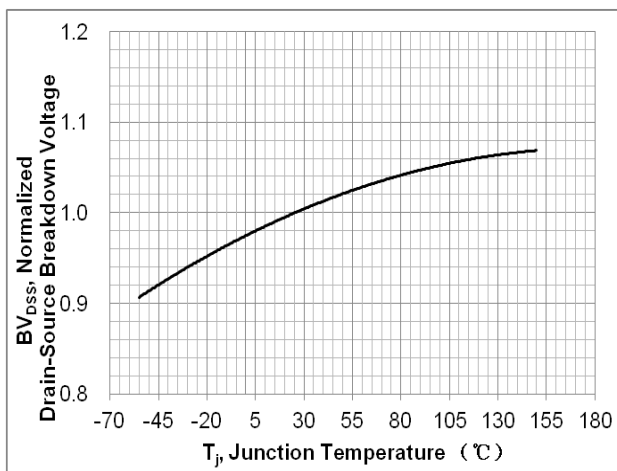
**Fig. 3. On-resistance variation vs. drain current and gate voltage**



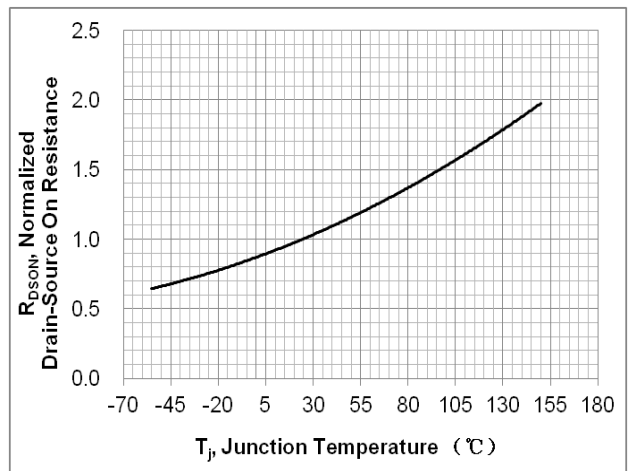
**Fig. 4. On-state current vs. diode forward voltage**



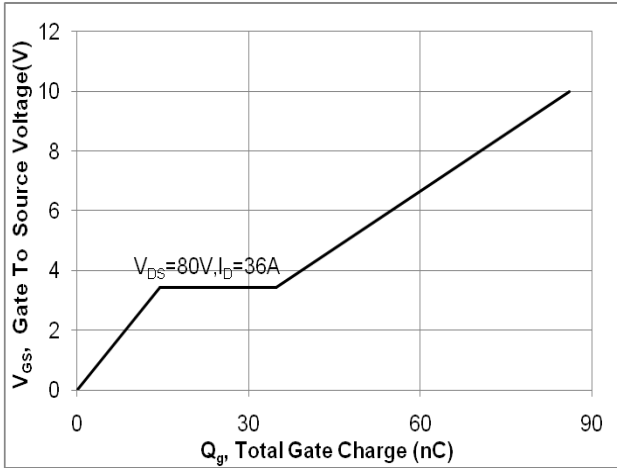
**Fig 5. Breakdown voltage variation vs. junction temperature**



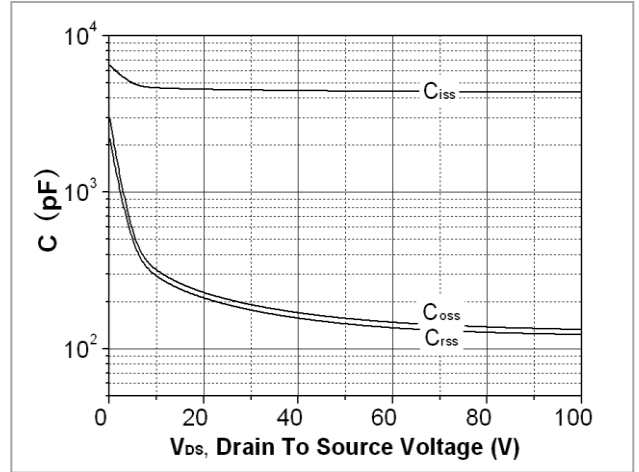
**Fig. 6. On-resistance variation vs. junction temperature**



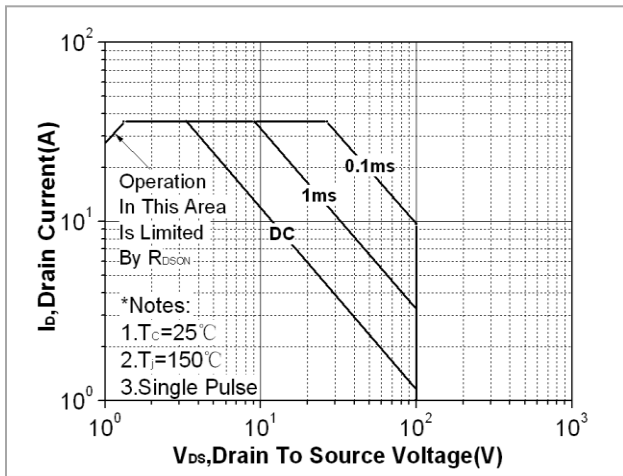
**Fig. 7. Gate charge characteristics**



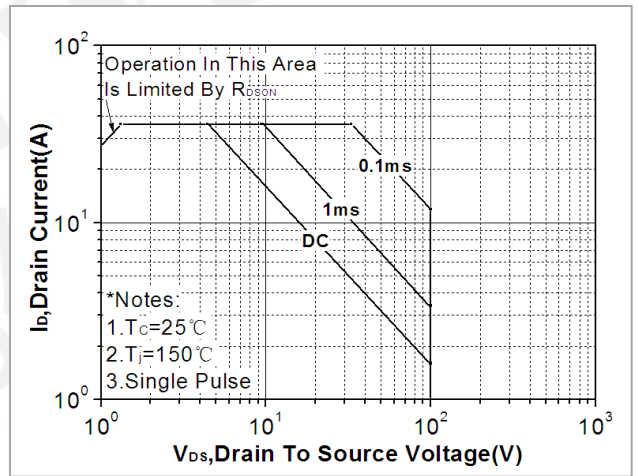
**Fig. 8. Capacitance Characteristics**



**Fig. 9. Maximum safe operating area(TO-252)**



**Fig. 10. Maximum safe operating area(TO-251)**



**Fig. 11. Maximum safe operating area(SOP-8)**

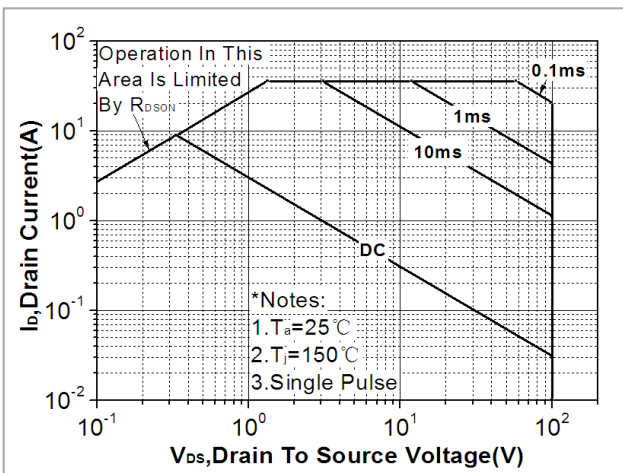


Fig. 12. Transient thermal response curve(TO-252)

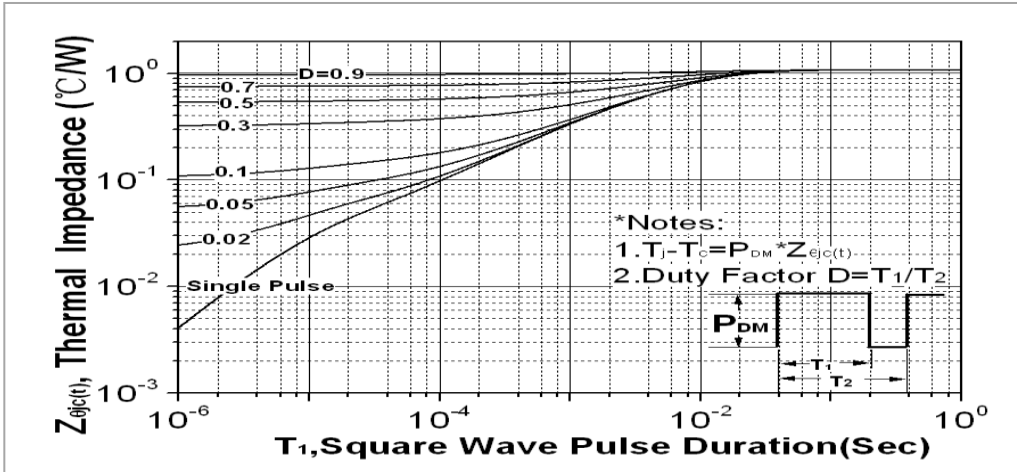


Fig. 13. Transient thermal response curve(TO-251)

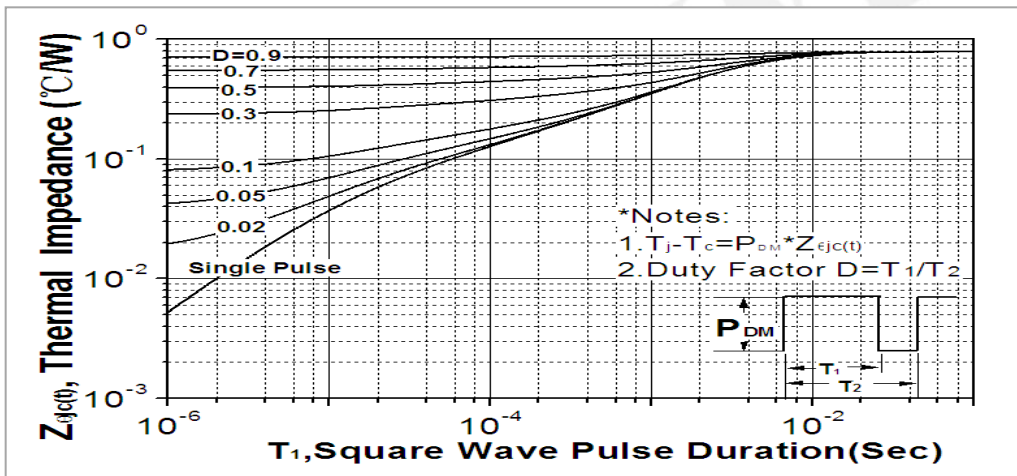
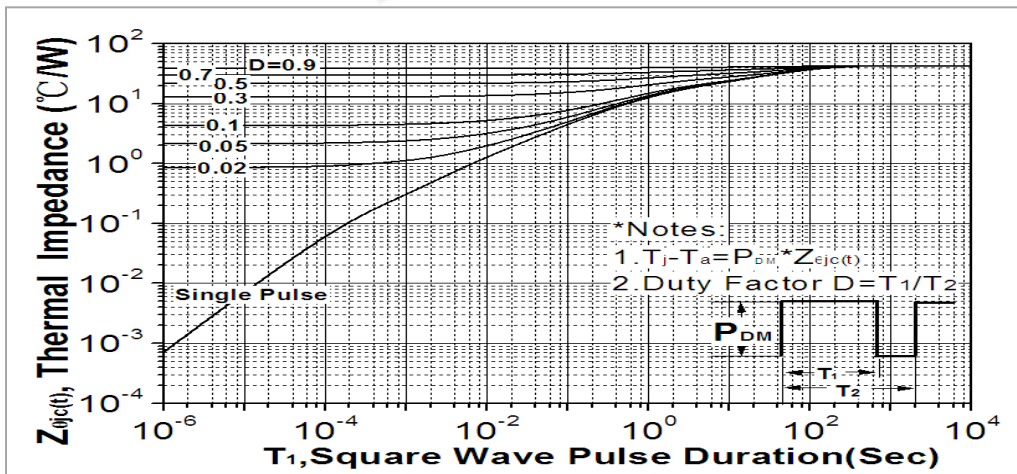
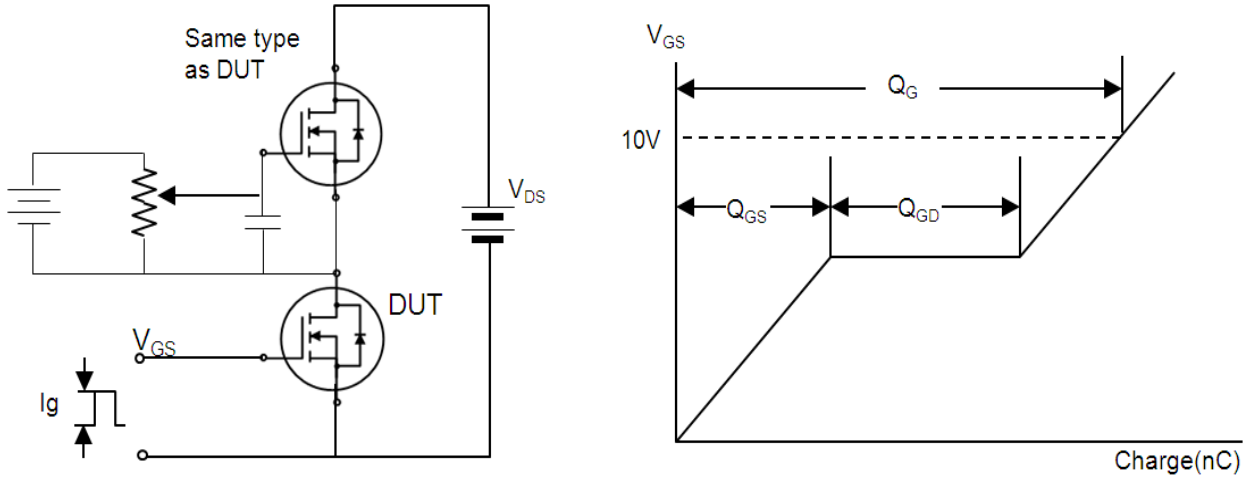


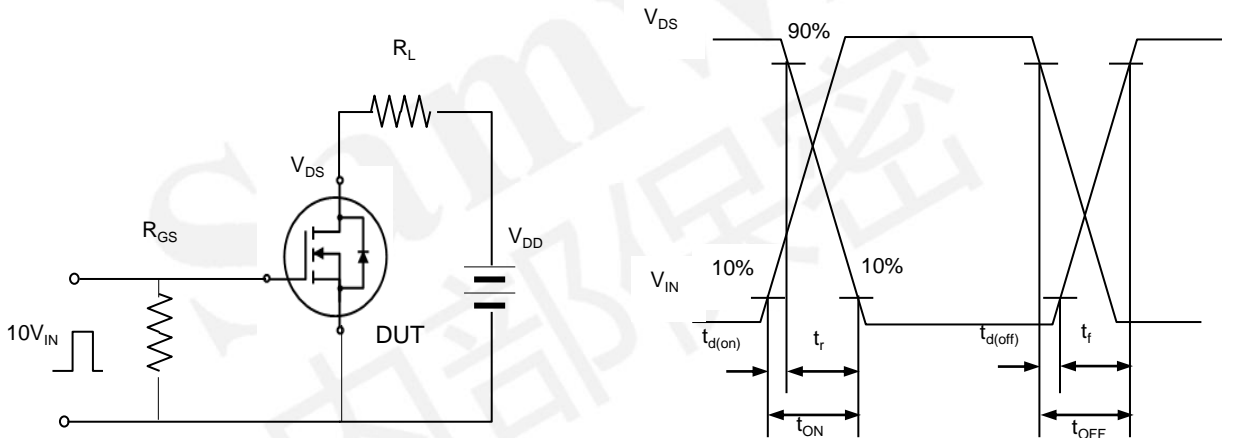
Fig. 14. Transient thermal response curve(SOP-8)



**Fig. 15. Gate charge test circuit & waveform**



**Fig. 16. Switching time test circuit & waveform**



**Fig. 17. Unclamped Inductive switching test circuit & waveform**

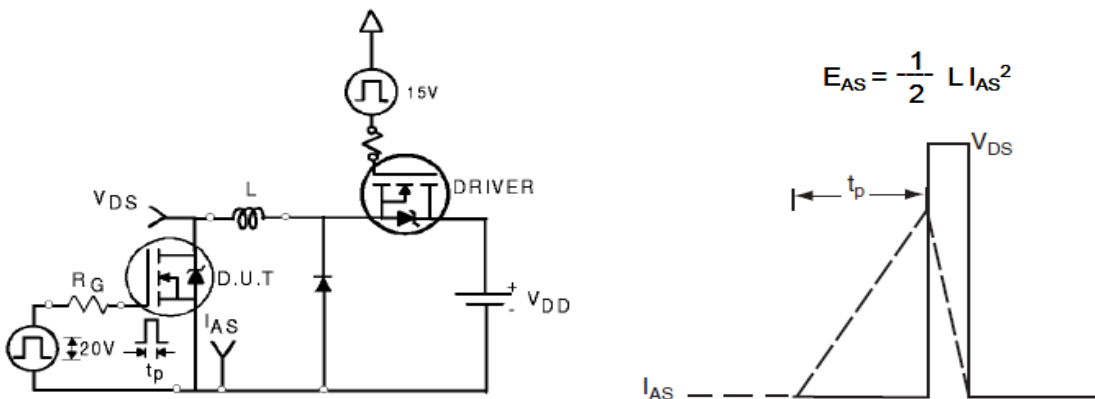
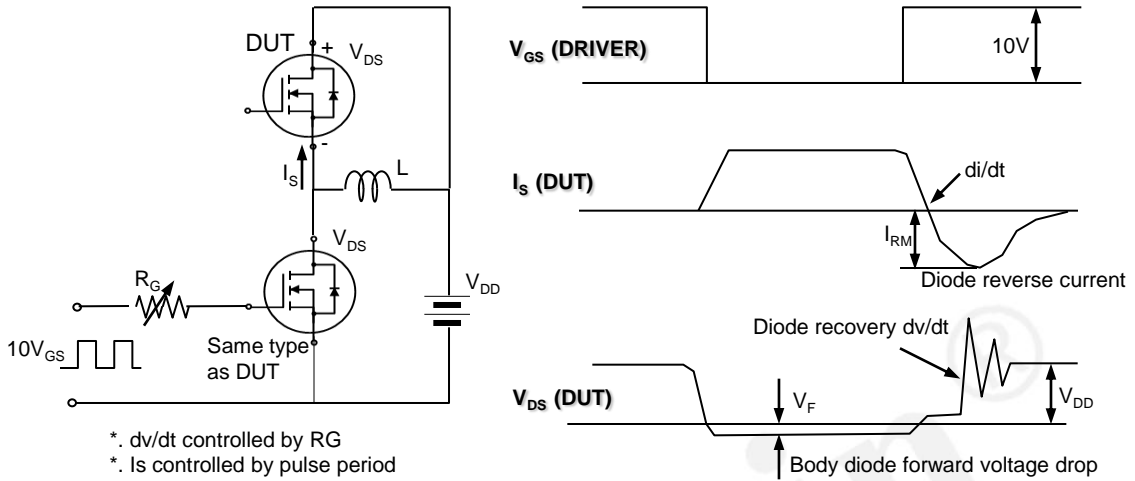


Fig. 18. Peak diode recovery dv/dt test circuit & waveform



### DISCLAIMER

\* All the data & curve in this document was tested in XI' AN SEMIPOWER TESTING & APPLICATION CENTE R.

\* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.

\* Qualification standards can also be found on the Web site (<http://www.semipower.com>)

\* Suggestions for improvement are appreciated, Please send your suggestions to [samwin@samwinsemi.com](mailto:samwin@samwinsemi.com)